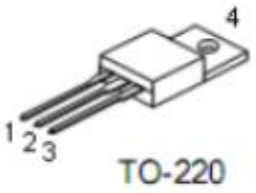
1. Applications

- High efficiency synchronous rectification in SMPS
- High speed power switching

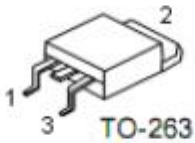
2. Features

- $R_{DS(on)}$=6.0mΩ @V_{GS}= 10 V
- Super high dense cell design
- Ultra low On-Resistance
- 100% avalanche tested
- Lead Free and Green devices available (RoHS Compliant)

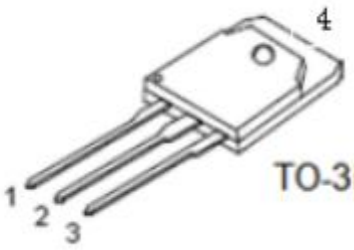
3. Pin configuration



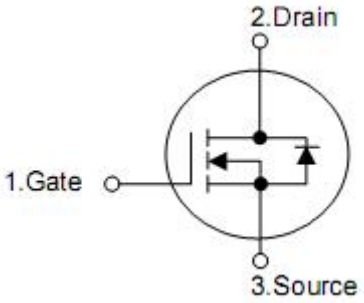
TO-220



TO-263



TO-3P



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Absolute maximum ratings

(T_C=25 ºC , unless otherwise specified)

Parameter		Symbol	Ratings		Units
			TO-220/263	TO-3P	
Drain-source voltage		V_{DSS}	100		V
Gate-source voltage		V_{GSS}	±25		V
Continuous drain currenet T_C=25 ºC[2]		I_D	130		A
Continuous drain currenet T_C=100 ºC[2]			99		A
300us pulsed drain current tested T_C=25 ºC[1]		I_{DP}	560		A
Avalanche energy single pulse[3]		E_{AS}	552		mJ
Power dissipation	T_C=25 ºC	P_D	300	375	W
	T_C=100 ºC		150	187.5	W
Maximum junction temperature		T_J	175		˚C
Storage temperature range		T_{STG}	-55~+175		˚C
Diode continuous forward current T_C=25 ºC		I_S	140		A

5. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance,Junction-to-case	θ_{JC}	0.5	ºC/W
Thermal resistance,Junction-to-ambient	θ_{JA}	62.5	ºC/W

6. Electrical characteristics

(T_C=25°C,unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off Characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	100	-	-	V
Drain-to-source leakage current	I_{DSS}	V_{DS}=100V ,V_{GS}=0V	-	-	1	μA
		T_J=125 °C	-	-	30	μA
Gate-to-source leakage current	I_{GSS}	V_{GS}=25V,V_{DS}=0V	-	-	100	nA
		V_{GS}=-25V,V_{DS}=0V	-	-	-100	nA
On characteristics						
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0	-	4.0	V
Static drain-source on-resistance[4]	$R_{DS(on)}$	V_{GS}=10V,I_D=40A	-	6.0	9.0	mΩ
Gate charge characteristics[5]						
Total gate charge	Q_g	V_{DS}=80V,I_D=70A,V_{GS}=10V	-	130	-	nC
Gate-source charge	Q_{gs}		-	32	-	
Gate-drain (Miller)charge	Q_{gd}		-	55	-	
Dynamic characteristics[5]						
Gate series resistance	R_G	V_{DS}=0V,V_{GS}=0V,f=1.0MHz	-	1	-	Ω
Turn-on delay time	$T_{d(ON)}$	V_{DD}=50V,I_D=70A,V_{GEN}=10V, R_G=5Ω	-	24	-	nS
Rise time	t_{rise}		-	91	-	
Turn-off delay time	$T_{d(OFF)}$		-	75	-	
Fall time	t_{fall}		-	65	-	
Input capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1.0MHz	-	6800	-	pF
Output capacitance	C_{oss}		-	630	-	
Reverse transfer capacitance	C_{rss}		-	350	-	
Source-drain body diode characteristics	T_J=25°C,unless otherwise notes					
Diode forward voltage[4]	V_{SD}	V_{GS}=0V,I_S=70A	-	-	1.2	V
Reverse recovery time	t_{rr}	I_{SD}=70A,di_F/dt=100A/μs,	-	43	-	ns
Reverse recovery charge	Q_{rr}		-	67	-	nC

Note: 1. Pulse width limited by safe operating area.

2. Caiculated continuous current based on maximum allowable junction temperature. The package limitation current is 75A

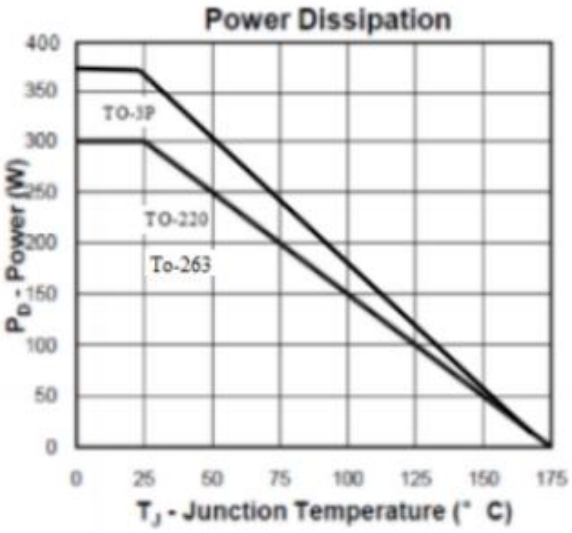
3. Limited by $T_{Jmax,}$ I_{AS}=47A, V_{DD}=48V, R_G=50Ω, Starting T_J=25°C.

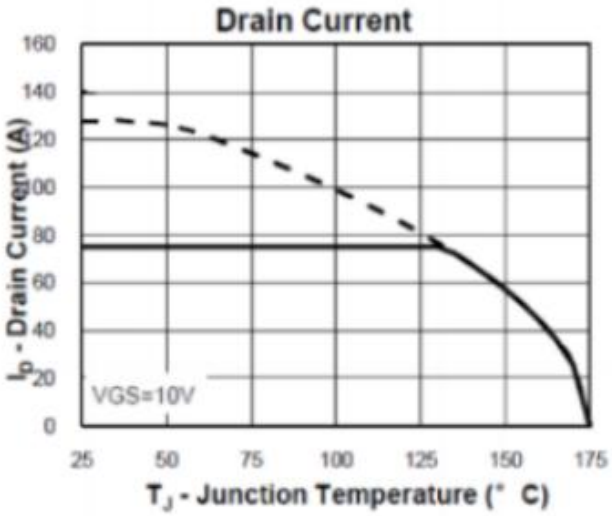
4. Pulse test; Pulse width ≤300μs; duty cycle ≤2%.

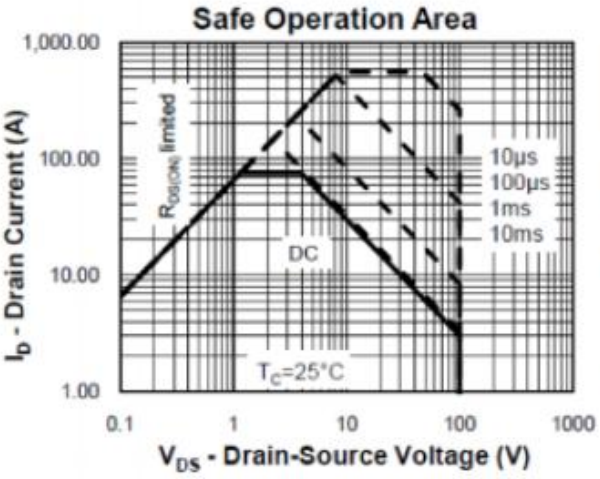
5. Guaranteed by design, not subject to production testing.

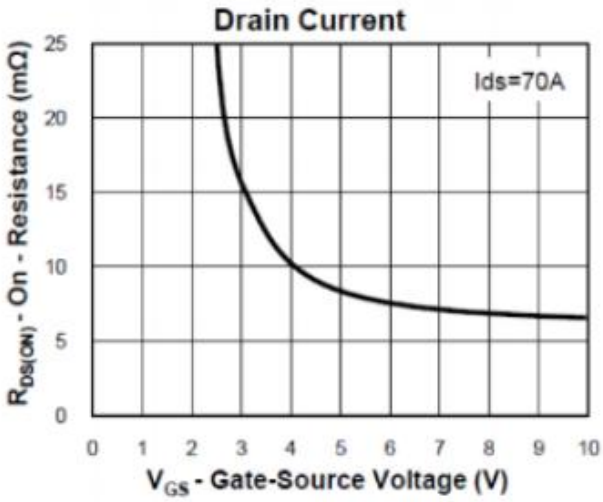
6.KIA finished product specifications please customer before placing order, should obtain the latest version of the finished product specifications.

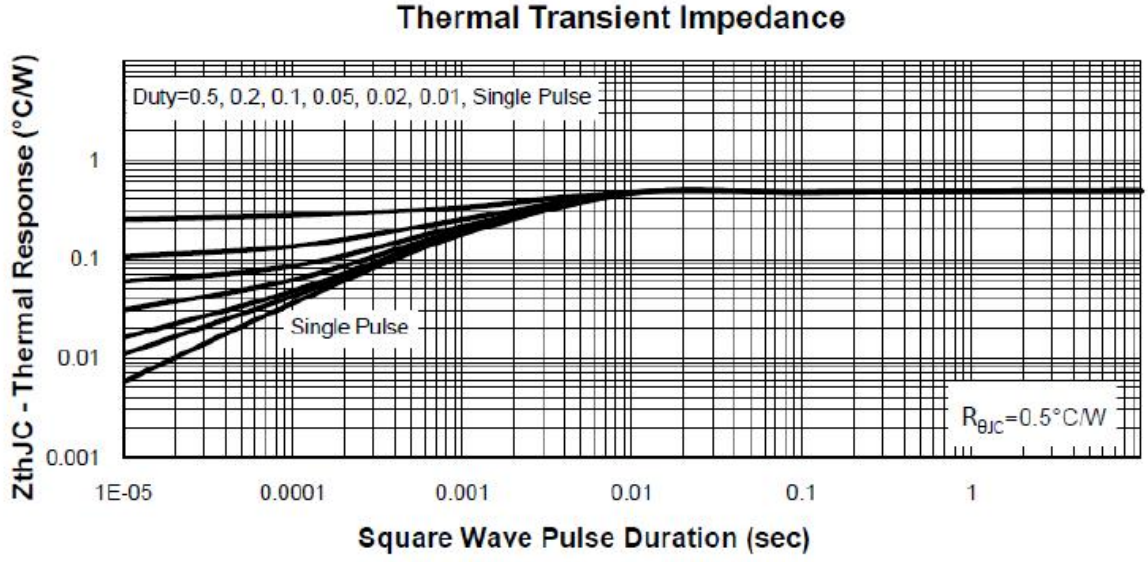
7. Typical characteristics

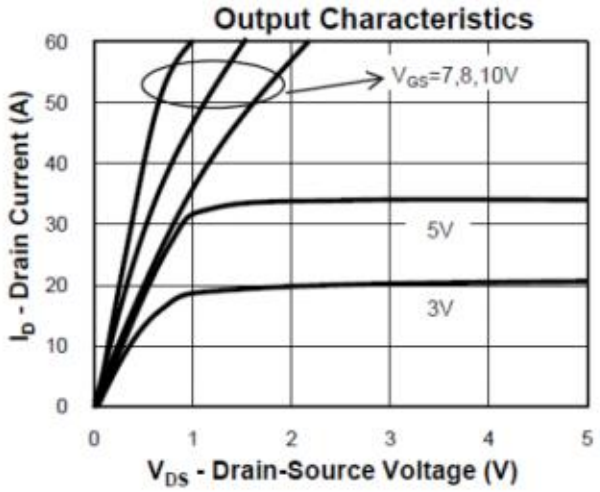


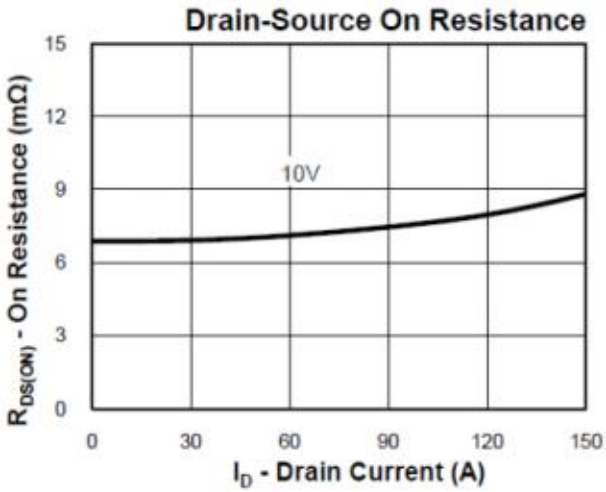


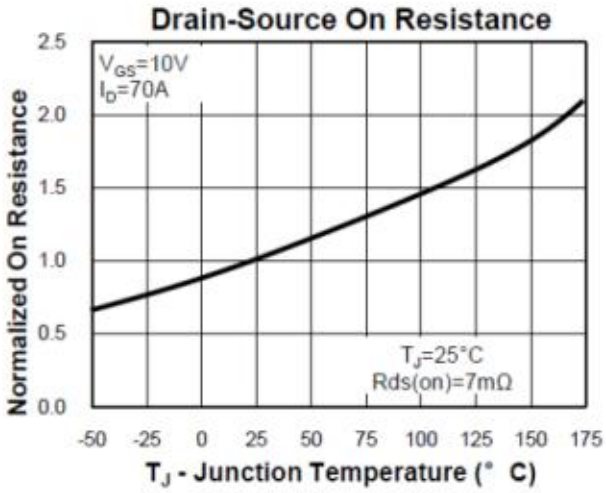


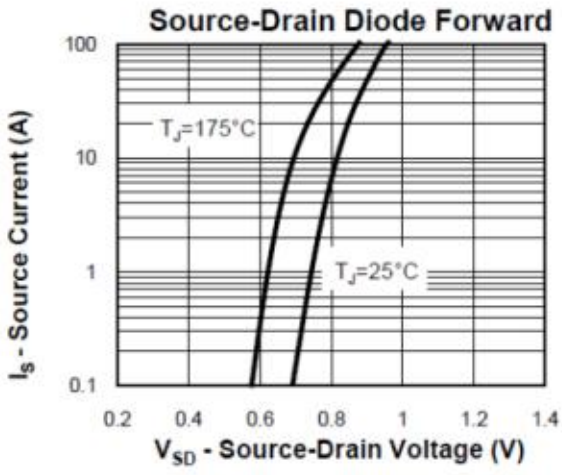


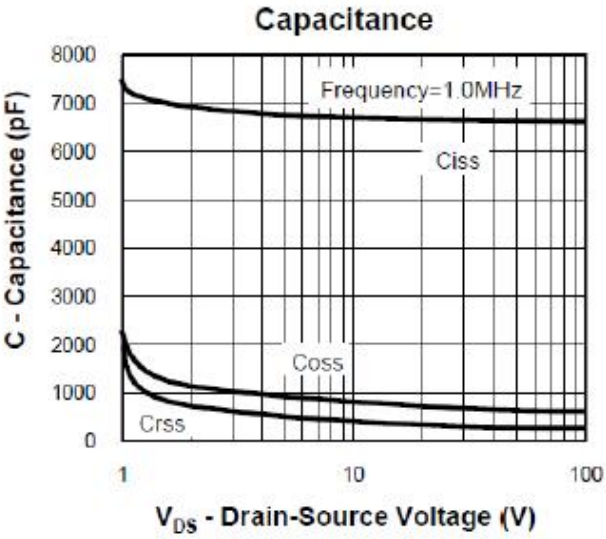


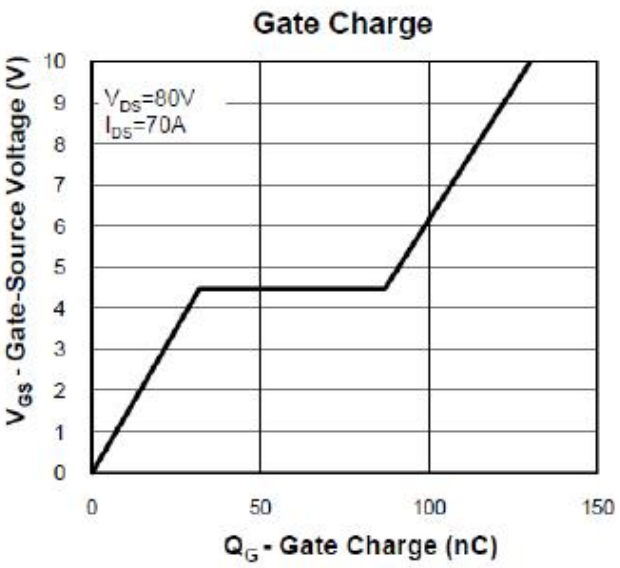

Output Characteristics
I_D - Drain Current (A)
V_{DS} - Drain-Source Voltage (V)
V_{GS}=7,8,10V
5V
3V


Drain-Source On Resistance
$R_{DS(ON)}$ - On Resistance (mΩ)
I_D - Drain Current (A)
10V


Drain-Source On Resistance
Normalized On Resistance
T_J - Junction Temperature (° C)
V_{GS}=10V
I_D=70A
T_J=25°C
Rds(on)=7mΩ

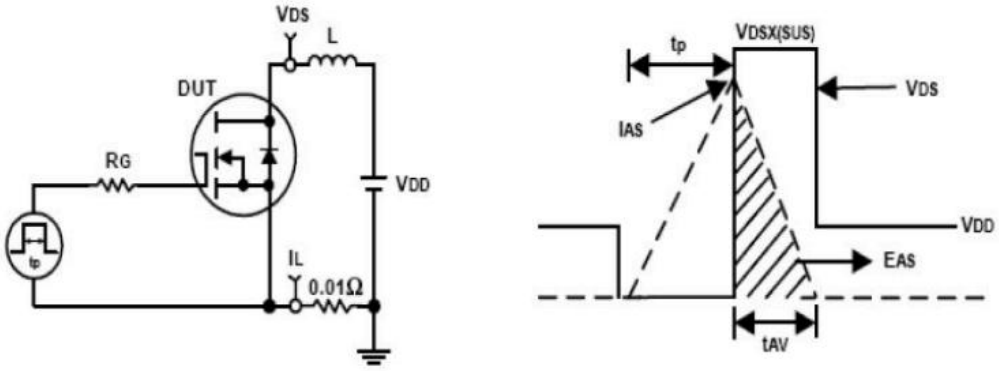

Source-Drain Diode Forward
I_S - Source Current (A)
V_{SD} - Source-Drain Voltage (V)
T_J=175°C
T_J=25°C


Capacitance
C - Capacitance (pF)
V_{DS} - Drain-Source Voltage (V)
Frequency=1.0MHz
Ciss
Coss
Crss


Gate Charge
V_{GS} - Gate-Source Voltage (V)
Q_G - Gate Charge (nC)
V_{DS}=80V
I_{DS}=70A

8. Test circuits and waveforms

Avalanche Test Circuit and Waveforms



Switching Time Test Circuit and Waveforms